FABRICATION, CHARACTERIZATION AND OPTIMIZATION OF IN-HOUSE MOSFET TRANSISTOR USING SPIN ON DOPANT TECHNIQUE

MARLIA BINTI MORSIN

KOLEJ UNIVERSITI TEKNOLOGI TUN HUSSEIN ONN

KOLEJ UNIVERSITI TEKNOLOGI TUN HUSSEIN ONN

BORANG PENGESAHAN STATUS TESIS♦

JUDUL: **FABRICATION, CHARACTERIZATION, AND OPTIMIZATION OF IN-HOUSE MOSFET TRANSISTOR USING SPIN ON DOPANT TECHNIQUE**

:

SESI PENGAJIAN: 2004/2005

Saya **MARLIA BINTI MORSIN**
(HURUF BESAR)

mengaku membenarkan tesis (~~PSM~~/ Sarjana/ ~~Doktor Falsafah~~)* ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Tesis adalah hakmilik Kolej Universiti Teknologi Tun Hussein Onn.
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.s
3. Perpustakaan dibenarkan membuat salinan tesis ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. **Sila tandakan (√)

☐	SULIT	(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)
☑	TERHAD	(Mengandungi maklumat TERHAD yang telah ditentukan oleh organisasi/ badan di mana penyelidikan dijalankan
☐	TIDAK TERHAD	

Disahkan oleh

(TANDATANGAN PENULIS)

Alamat Tetap:
No. 1, Jalan Bukit, Bukit Batu,
81020 Kulai, Johor.

Tarikh: **2 NOVEMBER 2004**

(TANDATANGAN PENYELIA)

PROF. DR. HASHIM BIN SAIM
(Nama Penyelia)

Tarikh: **2 NOVEMBER 2004**

CATATAN:
* Potong yang tidak berkenaan.
** Jika tesis ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa organisasi berkenaan dengan menyetakan sekali sebab dan tempoh tesis ini perlu dikelaskan sebagai SULIT atau TERHAD.
♦ Tesis dimaksudkan sebagai tesis bagi Ijazah Doktor Falsafah dan Sarjana secara penyelidikan, atau disertasi bagi pengajian secara kerja kursus dan penyelidikan, atau Laporan Projek Sarjana Muda (PSM).

"This thesis has been read and certified by".

SIGNATURE	:	.....
SUPERVISOR I	:	**PROFESSOR DR. HASHIM BIN SAIM**
DATE	:	**2 NOVEMBER 2004**

SIGNATURE	:	.....
SUPERVISOR II	:	**ASSOCIATE PROFESSOR DR. UDA BIN HASHIM**
DATE	:	**2 NOVEMBER 2004**

FABRICATION, CHARACTERIZATION AND OPTIMIZATION OF IN-HOUSE MOSFET TRANSISTOR USING SPIN ON DOPANT TECHNIQUE

MARLIA BINTI MORSIN

This thesis is submitted in partial to fulfillment of the requirement for the
Master of Electrical Engineering

Faculty of Electrical and Electronic Engineering
Tun Hussien Onn University College of Technology

NOVEMBER, 2004

"Hereby, I declare that this thesis entitled "Fabrication, Characterization, and Optimization of In-House MOSFET Transistor using Spin - On Dopant Technique" is a result of my own research and idea except for the work that has been clearly cited in the references".

SIGNATURE : .....

NAME : **MARLIA BINTI MORSIN**

DATE : **2 NOVEMBER 2004**

To Mak and Ayah; for your love and support
My bros and sis, together we fight and reach the top
And for me...one step closer to hit

ABSTRACT

This thesis explains the development and fabrication of first in-house MOSFET device using spin –on dopant technique at KUKUM Microfabrication Cleanroom. The process started with the establishment of process flow, process modules, and process parameters. Four modules were developed. The characteristics prior to the MOSFET device fabrication namely dry and wet oxidation, etching, resist thickness, exposure dose optimization, n-type and p-type spin on dopant and diffusion and also metal thickness characterization were recorded. The data were analyzed and applied in the fabrication of MOSFET devices. The MOSFET fabrication process used blanket-field oxide for isolation, positive resist for lithography process, Boron and Phosphorus for source/drain doping and aluminum for metallization. The whole MOSFET process had four masking process specifically source/drain masking, gate masking, contact masking, and metal masking. The result for each processes are presented in this thesis.

ABSTRAK

Tesis ini menerangkan mengenai pembangunan modul dan proses fabrikasi peranti MOSFET yang pertama dibina menggunakan teknik "spin –on dopant" di Bilik Bersih, Makmal Mikrofabrikasi, KUKUM. Proses ini bermula dengan membangunkan aliran proses fabrikasi, modul proses and mengenalpasti paramater- parameter yang terlibat. Empat modul telah dibangunkan sebelum proses fabrikasi peranti MOSFET iaitu pengoksidaan basah dan kering serta punaran, ketebalan rintang foto dan pengoptimuman dos dedahan, resapan jenis n dan jenis p serta penglogaman. Setiap data dianalisa dan hasilnya digunakan di dalam proses fabrikasi MOSFET. Proses fabrikasi MOSFET menggunakan pengoksidaan selimut - medan untuk pengasingan transistor, rintang foto positif bagi proses lithografi, boron dan fosforan sebagai dopan untuk proses resapan dan aluminum bagi proses penglogaman. Keseluruhan proses ini melibatkan empat jenis topeng ; topeng telaga (salir dan sumber), topeng get, topeng tingkap sentuhan dan topeng logam. Hasil bagi setiap proses dinyatakan di dalam tesis ini.

ACKNOWLEDGEMENT

First of all, I would like to thank my project supervisors, Prof. Dr. Hashim bin Saim and Ass. Prof. Dr. Uda bin Hashim for providing me guidance and dedications to carry out this project.

I would like to express my sincere gratitude to Nurhamidah, Teaching Engineer and all staffs at School of Microelectronic Engineering, KUKUM and not forgotten to all staffs at Pusat Pengajian Siswazah, KUiTTHO for their valuable contribution and help.

Lastly, to all my beloved friends who were involved in this project whether directly or indirectly. Special thanks for all of you.

CONTENTS

CHAPTER	TITLE	PAGE
	TITLE	i
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENT	vii
	LIST OF TABLES	xi
	LIST OF FIGURES	xii
	LIST OF SYMBOL	xvi
	LIST OF APPENDIX	xviii
I	**PROJECT OVERVIEW**	1
	1.1 Overview	1
	1.2 Introduction	1
	1.3 Project Aspire	5
	1.4 Objective	5
	1.5 Project Scope	6
	1.6 Project Workflow	6

	1.7	Importance of the Project	7
II	**LITERATURE REVIEW – MOSFET TRANSISTOR**		9
	2.1	Overview	9
	2.2	Introduction	9
	2.3	MOSFET Device	12
	2.4	P- Channel MOSFET (PMOS)	13
		2.4.1 Structure of P-Channel MOS (PMOS) Transistor	14
		2.4.2 A Qualitative Description of P – Channel MOS (PMOS) Transistor Operation	16
	2.5	N- Channel MOSFET (NMOS)	19
		2.5.1 Structure of N-Channel MOS (NMOS) Transistor	19
		2.5.2 A Qualitative Description of N – Channel MOS (NMOS) Transistor Operation	20
	2.6	Geometric and material properties of a MOS transistor	23
		2.6.1 The gate capacitance	25
		2.6.2 Mobility of carriers	25
		2.6.3 DC analysis of the PMOS transistors	26
		2.6.3.1 Current-Voltage relationships	26
III	**LITERATURE REVIEW - FABRICATION PROCESS**		28
	3.1	Overview	28
	3.2	Introduction	28
	3.3	Wafer Preparation	29
		3.3.1 Doping Semiconductor	31
	3.4	Clean Process	33

3.4.1 Wet Cleaning Process 34

3.4.2 Contaminants 35

3.5 Thermal Process 35

3.5.1 Oxidation 35

3.5.1.1 Oxide Measurements 39

3.5.2 Diffusion 40

3.5.2.1 Deposition and Drive-In 45

3.5.2.2 Doping Measurement 45

3.6 Photolithography 47

3.6.1 Photoresist Coating 48

3.6.1.1 Photoresist 49

3.6.2 Soft Bake 51

3.6.3 Alignment and Exposure 52

3.6.3.1 Exposure source 52

3.6.4 Development 53

3.6.5 Hard Bake 54

3.6.6 Pattern Inspection 54

3.7 Etching 55

3.7.1 Wet Etch Process 56

3.7.1.1 Oxide Wet Etch 57

3.7.1.2 Metal Etch 58

3.7.2 Etch Basics 59

3.7.2.1 Etch Rate 59

3.7.2.2 Uniformity 59

3.8 Metallization 60

3.8.1 Aluminum 61

3.8.2 Physical Vapor Deposition (PVD) 62

3.8.2.1 Thermal Evaporation 62

3.8.2.2 Thickness Measurement 64

3.9 Characterization 65

IV	**METHODOLOGY**		66
	4.1	Overview	66
	4.2	Introduction	66
	4.3	Cleanroom	67
	4.4	Process equipment	70
	4.5	Consumables	81
V	**PROCESS MODULE DEVELOPMENT**		84
	5.1	Overview	84
	5.2	Introduction	84
	5.3	Oxidation	85
		5.3.1 Dry Oxidation	86
		5.3.2 Wet Oxidation	88
	5.4	Photolithography	90
	5.5	Diffusion	93
	5.6	Metallization	95
	5.7	Result and Discussion	96
		5.7.1 Oxidation	97
		5.7.2 Photolithography	101
		5.7.3 Diffusion	104
		5.7.4 Metallization	106
	5.8	Conclusion	108
VI	**THE FABRICATION PROCESS OF PMOS AND NMOS TRANSISTORS**		109
	6.1	Overview	109
	6.2	Methodology	109
		6.2.1 Fabrication Process of MOSFET (NMOS and PMOS Transistor)	110

VII	**RESULT AND DISCUSSION**		131
	7.1	Overview	131
	7.2	Result and discussion	132
	7.3	Summary	146
VIII	**CONCLUSION**		147
	8.1	Overview	147
	8.2	Conclusion	147
	8.3	Problem	148
	8.4	Future Suggestion	149
	REFERENCES		151

LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	Fundamental DC relationships for MOS transistors	26
4.1	A list of equipment	70
4.2	A list of consumables	81
5.1	Modules of MOSFET fabrication process	85
5.2	Process sequence summary of dry oxidation	87
5.3	Process sequence summary of wet oxidation	89
5.4	The program of Spin Processor (WS-400A-6NPP/LITE/IND)	91
5.5	Process sequence summary of Experiment 1	91
5.6	Process sequence summary of Experiment 2	92
5.7	Process sequence summary of Diffusion	94
5.8	Three phases of the deposition process	95
5.9	Process sequence summary of metallization	96
6.1	Modules of MOSFET fabrication process and its tasks	110
6.2	Process flow of MOSFET Fabrication Process	114
7.1	The specifications of wafers	132
7.2	The measurement of sheet resistance in diffusion process	135
7.3	Device and process parameters for NMOS and PMOS	146

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
1.1	The first transistor made by germanium was demonstrated on Dec. 23, 1947, at Bell Labs	2
1.2	Project Flow Chart	7
2.1	The family of transistor	11
2.2	(a) NMOS symbol and (b) PMOS symbol	12
2.3	Cross section and circuits symbols of (a) p – channel enhancement mode MOSFET and (b) p – channel depletion mode MOSFET.	14
2.4	An internal structure of a p – channel MOS transistor.	15
2.5	A p – channel MOS transistor under bias in the inversion region.	17
2.6	Typical behavior of drains current versus gate – source voltage for PMOS transistor	18
2.7	I_{DS}-V_{DS} characteristics for PMOS transistor	18
2.8	Cross section and circuits symbols of (a) n – channel enhancement mode MOSFET and (b) n – channel depletion mode MOSFET.	19
2.9	An internal structure of a n – channel MOS transistor.	20
2.10	A n – channel MOS transistor under bias in the inversion region.	21

2.11	Typical behavior of drains current versus gate – source voltage for PMOS transistor	22
2.12	I_{DS}-V_{DS} characteristics for PMOS transistor	23
2.13	Geometry of the MOS transistor	24
3.1	The subcell of the single – crystal silicon lattice structure	30
3.2	The <100> orientation plane.	30
3.3	(a) N-type (Phosphorus) doped silicon and (b) its donor energy band	32
3.4	(a) P-type (Boron) doped silicon, (b) its acceptor energy band	33
3.5	Wafer clean process	34
3.6	Diffusion doping process	41
3.7	Patterned diffusion doping process	41
3.8	Four point probe	46
3.9	(a) Photoresist applying and (b) photoresist coating	49
3.10	Patterning process with negative and positive photoresists	50
3.11	Different Baking Methods	51
3.12	The three steps of the development process	53
3.13	Wet etch process	56
3.14	Wet etch profiles	57
3.15	Schematic of thermal evaporator	63
3.16	Schematic of a profilometer	64
4.1	The Micro fabrication cleanroom layout	67
4.2	A view at Micro Fabrication Cleanroom, KUKUM.	68
4.3	Various view of an oxidation furnace	71
4.4	The P-Type and N-Type Diffusion Furnace	72
4.5(a)	The photoresist spinner and its programmer	73
4.5(b)	The Hot Plate	73
4.5(c)	The Mask Aligner and Exposure System	74
4.6	The Physical Vapor Deposition (PVD)	74
4.7	Wet Etch Bench. From left (a) BOE tank, (b) Rinse tank with De-Ionized (DI) water pipe (c) Spinner (d) ALUM Etchant	75

	tank (e) Acetone bottle	
4.8(a)	The IV test System	76
4.8(b)	The Electrical Probe Station	77
4.8(c)	The Four Point Probe	77
4.8(d)	The Conduction Gauge	78
4.9(a)	The High Power Microscope	78
4.9(b)	The Low Power Microscope	79
4.9(c)	The Step Height Measurement System –Stylus Surface Profiler	80
4.9(d)	The Spectrophotometer –Filmetrics	80
4.10	(a) N type of 4″ silicon wafer <100> orientation and (b) P-type of 4″ silicon wafer <100> orientation	82
4.11	(a) Liquid dopant (Boron) ad (b) Liquid dopant (Phosphorus)	82
4.12	Positive Photoresist	83
4.13	(a) BOE- Buffered Oxide Etch solution, (b) Aluminum Etchant solution,(c) Acetone and (d) Developer	83
5.1	Dry Oxidation Furnace Set	87
5.2	Wet Oxidation Furnace Set	89
5.3	The growth rates for dry oxidation process	98
5.4	The growth rates for wet oxidation process	99
5.5	The growth rates for dry and wet oxidation processes	100
5.6	The etch rate of oxide thickness for both oxidation process	101
5.7	The photoresist thickness vs. spin speed with ramp up fixed to 800 rpm.	102
5.8	The standard deviation vs. spin speed.	102
5.9	The image of resist profile with different exposure times (a) 70 seconds (b) 80 seconds (c) 90 seconds (d) 100 seconds (e) 110 seconds	103
5.10	Graph of sheet resistance vs. temperature for Boron doping process in 60 minutes and 75 minutes.	104
5.11	Graph of sheet resistance vs. temperature for Phosphorus doping process in 15 minutes and 20 minutes.	105

5.12	Graph of aluminum thickness vs. size of aluminum.	106
5.13	The graph of sheet resistance vs. size of aluminum	107
5.14	The five point set on the cutting wafer	107
5.15	Graph of aluminum thickness vs. time	108
7.1	The inspection outcome on P1 wafer in source/drain masking process.	133
7.2	The inspection outcome on N1 wafer in source/drain masking process.	134
7.3	The inspection outcome on P1 wafer in gate masking process.	136
7.4	The inspection outcome on N1 wafer in gate masking process.	137
7.5	The inspection outcome on P1 wafer in contact masking process.	139
7.6	The inspection outcome on N1 wafer in contact masking process.	140
7.7	The inspection outcome on P1 wafer in metal masking process.	142
7.8	The inspection outcome on N1 wafer in metal masking process.	143
7.9	I_{DS}-V_{DS} characteristics for PMOS transistor	144
7.10	I_{DS}-V_{DS} characteristics for NMOS transistor	144
7.11	(a) The PMOS transistors (b) The NMOS transistors	145

LIST OF SYMBOL

a	Lattice parameter
A	Constant in oxidation law
Å	Symbol for 10^{-10}cm or 10^{-8}m
B	Constant in oxidation law
β	Linear gain
C	Capacitance per unit area
C_{ox}	Oxide capacitance per unit area
D	A dopant (chemical equation only)
D	Diffusion coefficient
g_m	Transconductance
h	Planck's constant
I	Current
I_B	Body current
I_D	Drain current
I_G	Gate current
I_S	Source current
j	Flux
k	Boltzmann's constant
k	Segregation coefficient
l	A length
m	Mass
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

NMOS	N- Channel Metal Oxide Semiconductor
PMOS	P- Channel Metal Oxide Semiconductor
q	Charge on the electron
Q	Charge per unit area
t	Time
t_{ox}	Oxide thickness
V_B	Body voltage
V_D	Drain voltage
V_{DS}	Drain – Source Voltage
V_G	Gate voltage
V_{GS}	Gate-Source Voltage
V_{TH}	Threshold voltage
W	Work function of metal
x_i	Initial oxide thickness
x_j	Junction depth
x_o	Thickness of oxide film
X	Property of material
ε	Permittivity
ε_o	Permittivity of free space
ε_{ox}	Permittivity of silicon dioxide
μ	Mobility
μ_n	Electron mobility
μ_p	Hole mobility
ρ	Charge distribution
ρ	Resistivity
ρ_s	Sheet resistivity
R_s	Sheet resistance
Ω	Symbol for ohms

LIST OF APPENDIX

APPENDIX NO.	TITLE	PAGE
A	The first PMOS and NMOS fabrication process	1
B	Process Module Development	4
C	Fabrication process of PMOS and NMOS transistors	28

CHAPTER I

PROJECT OVERVIEW

1.1 Overview

This chapter will explain the project overview including objective, scopes, and methodology of project.

1.2 Introduction

The rise of MOS technology is a classic study since it is the most important devices in electronic industry [1] due to its capability. This project is stressed on the fabrication, characterization, and optimization of in-house MOSFET devices. In order to fabricate the devices, the process module development was established and formed backbone of this project.